LXI Consortium

Implementing IEEE 1588 in LXI

John C. Eidson

john_eidson@agilent.com

LAN eXtensions for Instrumentation

www.lxistandard.org

Agenda

- LXI and IEEE 1588 context
- Where to get help
- What is IEEE 1588?
- IEEE 1588 features and implementation
- Coupling IEEE 1588 to your instrument

LXI and IEEE 1588 context

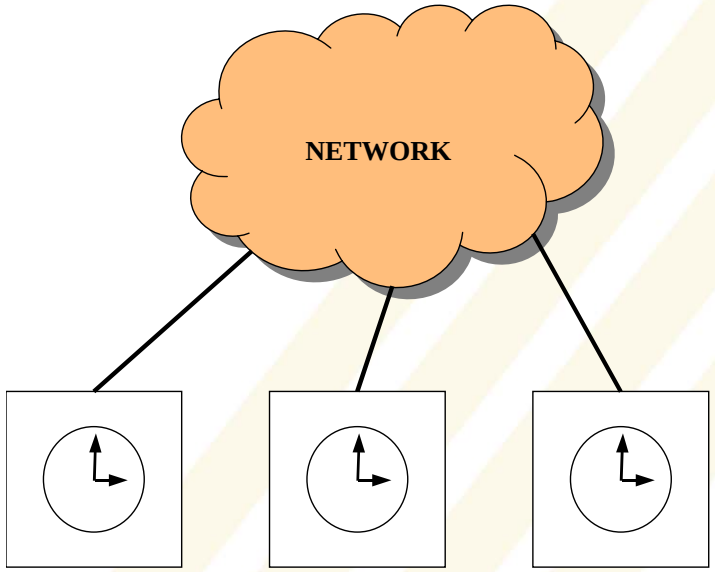
- LXI standard, section 3
  - 3.2 Rule “Each LXI device that complies with LXI Class A or LXI Class B shall provide fully conformant IEEE Std 1588 Precision Time Protocol functionality”
- In an LXI system, IEEE 1588 provides a common sense of precise time in all Class A & B devices that can be used by system integrators to control the system and to manage the data.

Where to get help

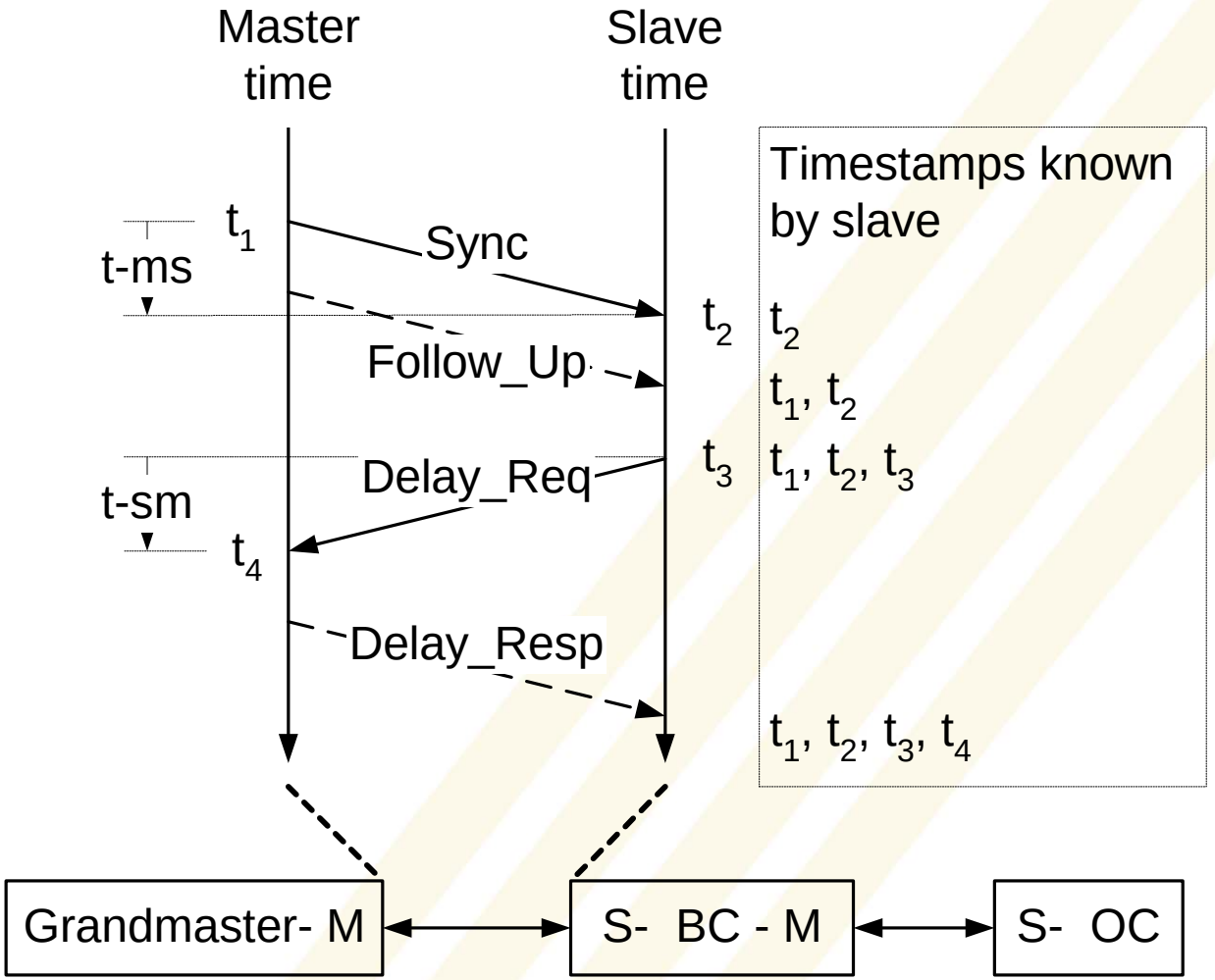
- IEEE 1588 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems.
- Also known as IEC 61588
- Version 2 is in ballot process
- Available from IEEE as 61588-2004, see http://ieeexplore.ieee.org/Xplore/dynhome.jsp
- IEEE 1588 web site, see http://ieee1588.nist.gov
  - Publications, products, conferences

What is IEEE 1588?

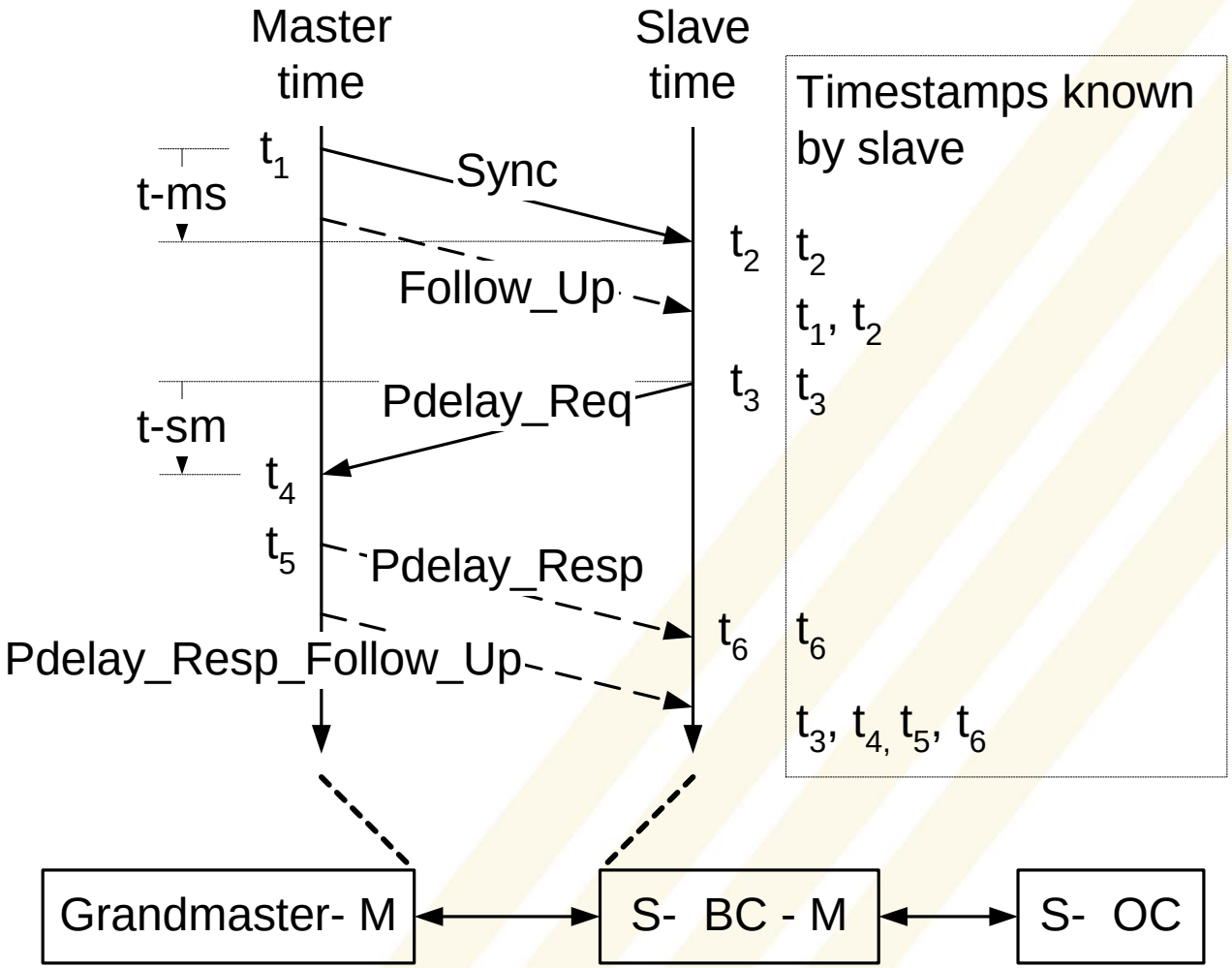
- IEEE 1588 is a protocol for accurately synchronizing clocks in a distributed system
- It does NOT say how to use these clocks
- The LXI standard says how to use them in an instrument system



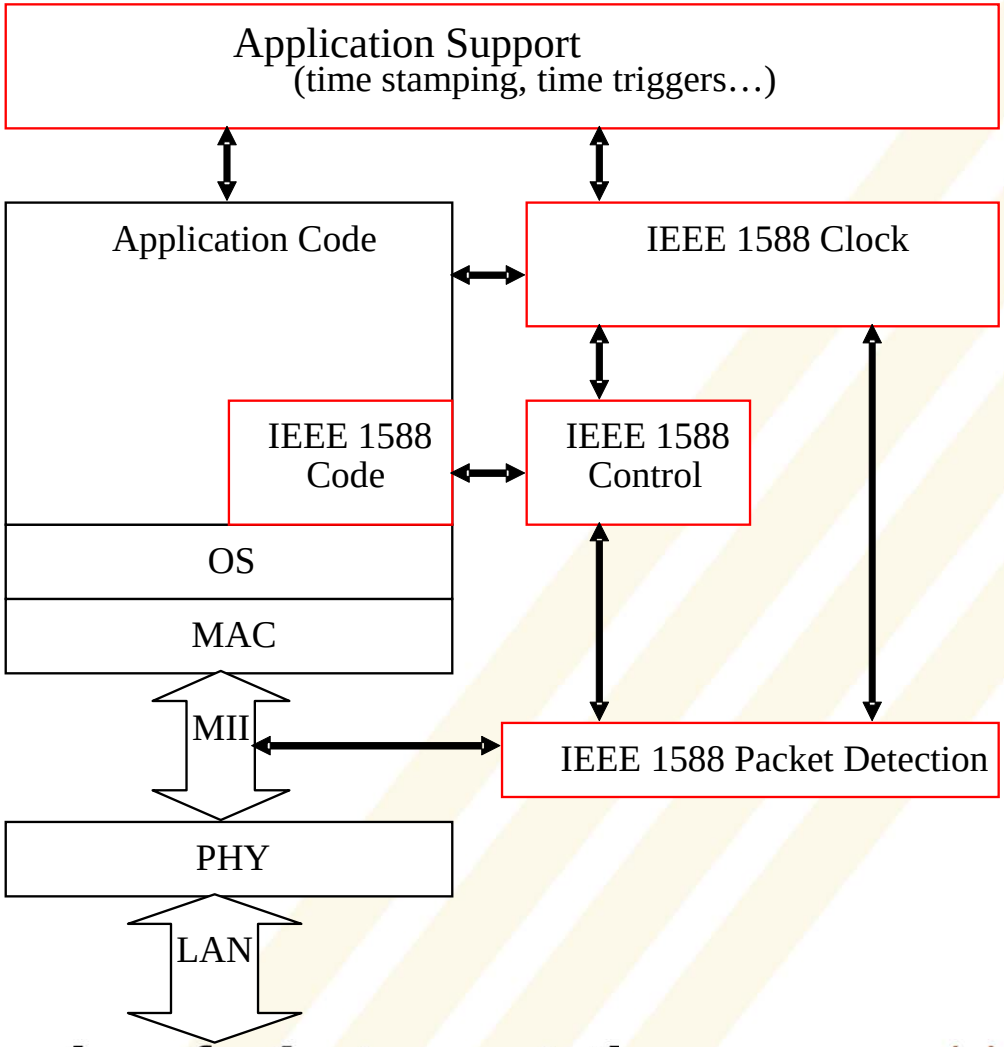
IEEE 1588 features and implementation (basic 'end-to-end' operation)



IEEE 1588 features and implementation
(basic 'peer-to-peer': probably not used in LXI)



IEEE 1588 features and implementation (typical architecture)



IEEE 1588 features and implementation
(IEEE 1588 functions)

- Determine master-slave hierarchy (software)
- Timestamp generation (hardware or software)
- Timing messages (software)
- Clock synchronization (software/hardware)
- Clock and system configuration and management (software)

IEEE 1588 features and implementation
(General software guidelines)

- Almost all messages are transmitted as multicast to standard port numbers and addresses (port 319, 320 and address 224.0.1.129)
- Most 1588 code is not time-critical (unless you generate timestamps at the ISR)
- Pay particular attention to matching hardware generated timestamps and packets on the protocol stack
- Watch roll-over of the clock and sequence numbers

IEEE 1588 features and implementation
(Determine master-slave hierarchy)

- Distributed algorithm (best master clock algorithm) based on multicast “Announce” messages
- Announce messages contain attributes
  - Priority
  - Class (TAI traceable time?)
  - Accuracy (how close is time to TAI?)
  - Variance (stability and noise of local clock)
  - UUID
  - Path information (how far to the grandmaster?)

IEEE 1588 features and implementation (Determine master-slave hierarchy)

Best master clock algorithm.

A typical instrument named A:

- Sends Announce messages with attributes of A
- Receives Announce messages from others
- Compares attributes of received Announce messages with attributes of A
  - If A is ‘better’: keep sending Announce messages and become a master
  - If another instrument is ‘better: stop sending Announce messages and become a slave

IEEE 1588 features and implementation (Timing messages)

Event messages:

- Sync, Delay_Req (Pdelay_Req, Pdelay_Resp)
- Are timestamped
- Carry time stamps and time related information

General messages:

- Follow_Up, Delay_Resp, (Pdelay_Resp_Follow_Up)
- Are NOT timestamped
- Carry time stamps and time related information

IEEE 1588 features and implementation (Timestamp generation)

- For high accuracy generate close to PHY
- Generate at start-of-frame in Ethernet
- Qualify (filter) by:
  - IPv4
  - Port 319
  - (for safety: messageType field in user space)
- To associate timestamp with packet capture
  - sequenceId
  - sourcePortIdentity
  - (for safety: domain and messageType)

IEEE 1588 features and implementation (Clock synchronization)

- Compute offset_from_master (standard tells you how based on timestamps in event messages)
- Adjust the rate and time of slave clocks to minimize offset_from_master
- How to do this is implementation specific:
  - Need a good servo or phase lock loop designer
  - Think about filtering and statistics on the input data to the servo.

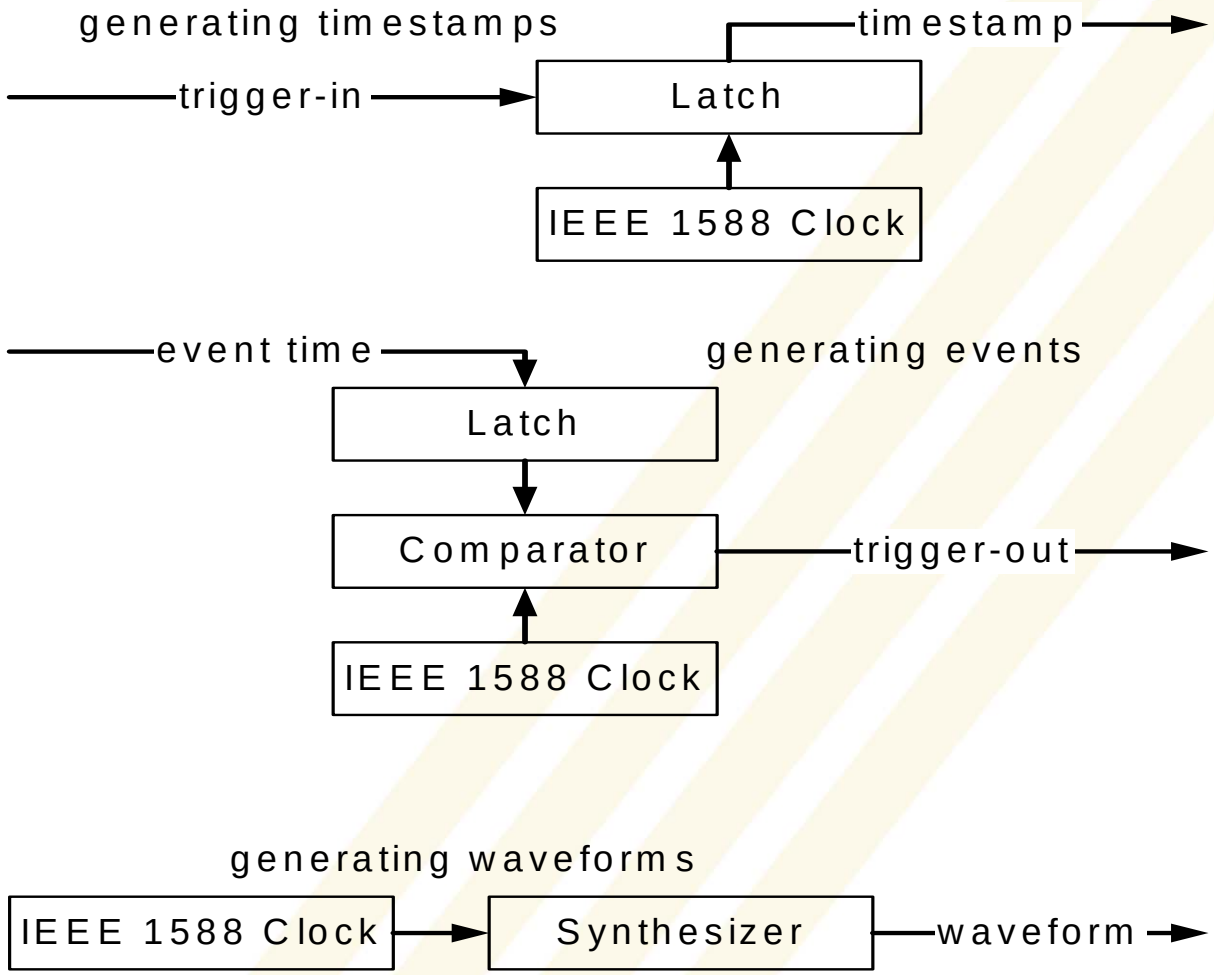
IEEE 1588 features and implementation (Clock and system management)

- IEEE 1588 specifies “management messages” to view and update data sets.
- These are simple to implement in an instrument (not so simple in a boundary clock)

Coupling IEEE 1588 to your instrument

- Implementing IEEE 1588 is the easy part
- Deciding how to use these clocks is where careful design is needed.
- Three general uses of synchronized clocks:
  - Timestamping data
  - Generating events (for example triggers)
  - Generating signals (for example periodic triggers, or waveforms synchronous with the clock)

Coupling IEEE 1588 to your instrument



Thank you.
Are there questions?